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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/523,239	09/28/2005	Franz Schuler	10808/206	6476

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EXAMINER	
SALERNO, SARAH KATE	
ART UNIT	PAPER NUMBER
2814	
MAIL DATE	DELIVERY MODE
11/03/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/523,239	SCHULER ET AL.	
	Examiner	Art Unit	
	SARAH K. SALERNO	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 October 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/21/10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on 10/21/10 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (JP 63-289853) in view of Tsukihara (JP 2000-269317) and Wu (US Patent 6,214,696)

Claim 1: Suzuki teaches a semiconductor component with trench isolation for defining active regions in a semiconductor substrate, the trench isolation comprising:

a deep isolation trench with a side wall insulation layer, an electrically conductive filling layer, which is electrically connected to a predetermined doping region (4) of the

semiconductor substrate (1) in a bottom region of the isolation trench further comprising: a trench contact which comprises: a deep contact trench with a side wall insulation layer (2) and an electrically conductive filling layer (3), which is electrically contact-connected to the predetermined doping region (4) of the semiconductor substrate (1) in a bottom region of the contact trench; a trench contact insulation layer (5) above a surface of the electrically conductive filling layer; a contact opening through the trench contact isolation layer in contact with the surface of the electrically conductive filling layer; and wherein a composition of the electrically conductive filling layer that is electrically, contact-connected to the predetermined doping region of the semiconductor substrate in a bottom region of the contact trench is the same as a composition of the electrically conductive filling layer having a top surface in contact with the contact opening (FIG. 1).

Suzuki does not teach a deep isolation trench with a first covering insulation layer below a surface of the semiconductor substrate and a second covering insulation layer over the first covering insulation layer and above the surface of the semiconductor substrate, a side wall insulation layer and an electrically conductive filling layer, and wherein the first covering insulation layer is over a top surface of the electrically conductive filling layer. Tsukihara teaches a deep isolation trench with a first covering insulation layer (30) below a surface of the semiconductor substrate and a second covering insulation layer (31) over the first covering insulation layer and above the surface of the semiconductor substrate (21), a side wall insulation layer (26) and an electrically conductive filling layer (28), and wherein the first covering insulation layer is

over a top surface of the electrically conductive filling layer; and Wu teaches a gate oxide layer (32) over a surface of the second covering insulation layer (28, first layer=26) to reduce parasitic capacitance in the trench isolation structure (ABS). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the trench isolation structure taught by Suzuki to contain the first and second insulation layer to reduce parasitic capacitance in the trench isolation structure s taught by Tsukihara (ABS).

Suzuki and Tsukihara do not teach a gate oxide layer over a surface of the second covering insulation layer. Wu teaches a gate oxide layer (32) over a surface of the second covering insulation layer (28, first layer=26) over a deep trench isolation for providing better insulating characteristics and improving latch-up immunity in the associated CMOS device (Col. 1). Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the device taught by Suzuki and Tsukihara to have a gate oxide layer over a surface of the second covering insulation layer of the deep trench isolation to have provided better insulating characteristics and improved latch-up immunity to the associated CMOS device as taught by Wu (Col. 1).

Claim 2: Tsukihara teaches the first covering insulation layer (10) is within the isolation trench (FIG. 2).

Claim 3: Suzuki teaches the trench isolation and the trench contact have a larger depth than an associated depletion zone in the semiconductor substrate (FIG. 2).

Claim 4: Tsukihara the trench isolation further comprises a widened, shallow isolation trench (29) at a surface of the semiconductor substrate configured for filling non-active regions to trench (FIG. 2).

Claim 5: Suzuki teaches the predetermined doping region comprises a doping well comprising a multiple well structure trench (ABS).

Claim 6: Suzuki, Tsukihara, and Wu teach the semiconductor substrate comprises Si (Wu 10), the covering insulation layer and side wall insulation layer comprise $Si0_2$ (Tsukihara 3), and the filling layer comprises highly doped polysilicon (Suzuki 3).

Response to Arguments

4. Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SARAH K. SALERNO whose telephone number is (571)270-1266. The examiner can normally be reached on M-R 8:00-4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Wael M Fahmy/
Supervisory Patent Examiner, Art Unit 2814

/S. K. S./
Examiner, Art Unit 2814